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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,646	07/27/2006	Albertus Jan Paulus Maria Van Uden	NL040064US1	9895

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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

NOTIFICATION DATE	DELIVERY MODE
12/05/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,646	VAN UDEN, ALBERTUS JAN PAULUS MARIA	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11 and 12* is/are rejected.

7)☒ Claim(s) *2-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *072706*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated July 27, 2006, claims 1-12 are active in this application.

Specification

2. If there are cross-reference to related applications, please include the respective patent numbers, if known.

Foreign Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statements filed July 27, 2006 have been considered.

Claim Objections

5. Claims 2-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections- 35 U.S.C. § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1 and 11 are rejected under 35 U.S.C 102(b) as being anticipated by Pascucci [U.S. Patent # 5,461,713].

With respect to claim 1, Pascucci disclose an integrated circuit device, comprising a read only memory matrix comprising cells organized in columns with associated bit lines and rows with associated word lines [see Detailed Description of the Invention], the matrix comprising data transistors coupled to both the bit lines and the word lines in data dependent ones of the cells; a differential sense amplifier [see figures, for example, figure 1a] having a first input [TPM], a second input [TPR] and a control input [TS] for controlling activation and deactivation of amplification by the sense amplifier a coupling circuit [CM] coupled between the bit lines and the first input for controllably permitting charge sharing between a selectable one of the bit lines and the first input a reference circuit coupled to the second input and arranged to controllably activate driving of a reference voltage at the second input; a timing circuit [see detailed description]

arranged to signal operation in a first phase, when the word lines have selected a row of the matrix, followed by a second phase, the timing circuit controlling the coupling circuit to permit charge sharing between the input and the selectable one of the bit lines in the first phase, and the timing circuit in the second phase controlling the coupling circuit to prevent said charge sharing, making the reference circuit deactivate driving the reference voltage, and activating amplification by the differential sense amplifier only when said charge sharing has been prevented and said driving has been deactivated. See detailed descripton.

With respect to claim 10, Pascucci discloses a precharge circuit [see 3rd paragraph of the Detailed Description of the Invention section] arranged to precharge the bit lines from a first power supply connection prior to said first phase and to decouple the bit lines from the first power supply connection during said second phase.

8. Claim 12 is rejected under 35 U.S.C 102(b) as being anticipated by Pascucci [U.S. Patent # 5,461,713].

With respect to claim 12, Pascucci discloses a method of reading data from a read only memory matrix in an integrated circuit device, the read only memory matrix comprising cells organized in columns with associated bit lines and rows with associated word lines the matrix [see Detailed Description] comprising data transistors [see figures and detailed description] coupled to both the bit lines and the word lines in data dependent ones of the cells; providing a differential sense amplifier [see figures] having a first input [TPM] a second input [TPR] and a control input [TS] for controlling

activation and deactivation of amplification by the sense amplifier [see detailed description] providing a coupling circuit [CM] coupled between the bit lines and the first input for controllably permitting charge sharing between a selectable one of the bit lines and the first input providing a reference circuit [CR] coupled to the second input the method comprising the following steps controllably activating the reference circuit to drive a reference voltage at the second input signaling operation in a first phase, when the word lines have selected a row of the matrix, wherein the coupling circuit is controlled to permit charge sharing between the input and the selectable one of the bit lines followed by a second phase, wherein the coupling circuit is controlled to prevent said charge sharing, making the reference circuit deactivate driving the reference voltage, and activating amplification by the differential sense amplifier only when said charge sharing has been prevented and said driving has been deactivated. See Detailed Description.

Allowable Subject Matter

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- the timing circuit comprises a dummy bit line capacitively loaded substantially as capacitive loading of a hypothetical bit line with a maximum number of data transistors coupled to that hypothetical bit line a dummy data transistor coupled to the dummy bit line a trigger circuit for triggering the second phase, the trigger circuit activating the dummy data transistor in the first phase and starting the

second phase when a potential swing on the dummy bit line due activation of the dummy data transistor in the first phase exceeds a threshold value larger than a potential swing that is needed on the bit line to cross the reference voltage.

- the reference circuit is local to a periphery of the memory matrix without containing signal lines that extend in parallel with the bit lines over a column height of the matrix.

- the differential sense amplifier is connected between a first and second power supply connection the sense amplifier comprising s first and second switching circuit coupled between the sense amplifier and the first and second power supply connection respectively the timing circuit deactivating and activating amplification by the sense amplifier by making both switching circuits non-conductive and conductive respectively.

- the reference circuit comprises a controllable equalization circuit coupled between the first and second input and arranged to equalize potentials on said first and second input prior to said first phase.

- the reference circuit comprises a PMOS bias transistor and an NMOS bias transistor with a main current channel coupled from the second input to a negative and a positive power supply terminal respectively, the timing circuit being arranged to drive the control electrodes of the PMOS bias transistor and the NMOS bias transistor to the potential of the negative and positive power supply terminal respectively during said first phase.

- the reference circuit comprises an first bias transistor and a second bias transistor of mutually opposite polarity with a main current channel coupled to respective power supply terminals the timing circuit being arranged to switch the main current channel of the first bias transistor to a conductive state and to switch the second bias transistor as a diode during said first phase.

- the timing circuit comprises a dummy bit line with a capacitive load substantially corresponding to a maximum possible capacitive load for any of the bit lines a pull transistor for pulling the potential of the dummy bit line starting from a the start of the first phase; a trigger circuit for triggering the second phase when the potential swing due to said pulling exceeds a threshold value larger than a potential swing that is needed on the bit line to cross the reference voltage.

Conclusion

10. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

11. .Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

12. .Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
December 3, 2008